
The Design of Filter Parameters of Dynamic Voltage Restorer in Medium Voltage Network

ABSTRACT: Dynamic Voltage Compensator (DVR) is able to handle the dynamic power quality problems in distribution network, such as voltage sags and voltage unbalance, and the parameters of the output filter will have important affect on the compensation results. In this paper, the parameter design method of the output filter of a cascaded H-bridge based DVR applied in medium-voltage distribution grid is studied. Through the analysis of the case when filter inductor current has the maximum value, the theoretical expression of the relationship between the low limit of the value of filter inductor and the capability of voltage compensation and power factor is derived. Meanwhile, the method of selecting the filter capacitor value is obtained. The realization of the proposed method are given by taking an engineering project as an example, the correctness and validity of the design method of filter parameters proposed in this paper are verified by simulation.

KEY WORDS: Dynamic voltage compensator; Filter parameters design; Output power factor;

0 Introduction

Dynamic Voltage Restorer (DVR) is a type of power quality control equipment connected in series between the distribution network and sensitive load to suppress the voltage sages. The coupling pattern between distribution network and DVR in medium voltage distribution network are mainly transformer coupling mode and capacitor coupling mode^[1]. The transformer coupling mode has the following disadvantages: the nonlinear characteristics of transformer itself can cause high harmonic distortion, and to overcome this will put forward higher requirements on the design of the transformer, thus increase the size and cost of the device^[2]; Other issues such as transformer saturation and the presence of instantaneous inrush current when voltage drops would threaten the safe operation of the system. When using capacitor coupling mode, it usually use the inductor in series with capacitor to form a low pass filter, and its parameters design is directly related to the quality of the output compensation voltage waveform, the dynamic response characteristics of DVR, and the cost and volume of DVR system. The output voltage harmonic components are the

main factor in affecting the quality of DVR compensation voltage waveform, in the PWM controlled inverter, usually there are two kinds of harmonic contents one is cause by the switching action of the inverter switching devices, and another is the harmonic introduced by nonlinear load and nonlinear factors such as the delay and death area of the inverter control pulses. A good design of LC filter should be able to limit the two kinds contents of harmonic components within a prescribed scope.

The design principle of the low-pass LC filter is that the cutoff frequency should be far more higher than the fundamental frequency of the network and be far more less than the lowest harmonic frequency in PWM voltage. Reference [2] calculates the product range of element L and C . Reference [3] carries out a large number of simulation analysis foe multilevel PWM inverter circuit, based on the analysis of the harmonic characteristic and considers the fundamental voltage drop, active power loss, current harmonic and resonance, derives the parameters of output filter, but its derivation process is simple, and only applies to DVR with special topology . In reference [4], the series of multilevel SPWM waveform is deduced and the accurate harmonic

spectrum is obtained. By computing high harmonic content and THD, theoretical basis is provided for the design of the filter. Based on this, factors such as the fundamental voltage drop on the filter inductor, current ripple, reactive power capacity are comprehensively considered, and the appropriate output filter parameters are designed. But the harmonic content analysis is not applicable to cascaded H-bridge topology. In Reference [5], the appropriate parameters of DVR LC filter are deduced by considering the load impedance. But this is for transformer coupling DVR system. Reference [6] studies the filter parameter value scope of DVR system under self-energized mode. In Reference[7], for the design of LC filter in large-capacity power electronics devices, the optimal control scheme of inverter called selective harmonic elimination pulse width modulation (SHE-PWM) is proposed. Based on the three-level neutral point clamped (NPC) inverter, the sub-synchronous SHE-PWM to ensure the resonance suppression that in the entire speed control range of the LC filter is used, and the method to design the LC resonant frequency is given. However, this method is suitable for large-capacity switching devices which operate at lower switching frequency, and is not suitable for high switching frequencies studied in this paper. In some studies on the capacitor coupling DVR of high-voltage large-capacity, only the value of the inductor or capacitor or the product range of the two parameters are given. Reference [8] presents a comprehensive tracking of reference voltage and effective damping of transient voltage oscillation sag compensation method, but the design of the filter parameters is not mentioned. Reference [9] uses parallel LC filter, and the inductor is connected between inverter and coupling transformer, three-phase parallel capacitor is in series with the same resistor, then is connected to the ground, the resistance is to prevent common mode disturbances in ground branch. This

structure can suppress resonance oscillation produced by series LC at high frequency, and can filter out the higher harmonics. However, the fundamental current of this kind of filter also flows through the inductor and will lead to an increase in volume of L . Reference [10] considers that the main role of the inductor of inverter is to weaken the output current ripple, and designs the value of the inductor of the converter side in accordance with ripple, the filter inductor and filter capacitor of grid side form a second-order filter, then filter out switching frequency harmonics of network current to meet the requirement of network, and this reference does not clarify in detail how the filter inductor and filter capacitor of the grid side design independently.

This paper presents a compensation scheme using DVR to compensate voltage sags in neutral-isolated medium voltage distribution network. The DVR is based on cascaded H-bridge and coupled with the network by LC low-pass filter, and the design of the parameters of LC filter is studied in detail. The design of lower value limit of the filter inductor is based on the peak of output current. The theory expression of lower value limit of the filter inductor by using two independent variables, i.e. the DVR maximum compensation voltage and output power factor, is derived, c. Filter capacitor value is calculated based on the constraint conditions that resonant frequency of the LC filter is much larger than the system frequency and far less than the switching frequency. Simulation results show that the design of the LC filter not only fully meet the system performance requirements, but also effectively reduce the cost and size of the filter.

1 The structure of DVR in 10kV network

As shown in Fig.1, a 10kV regional compensation Dynamic Voltage Restorer (DVR)

includes energy storage unit, an inverter, a filter coupling unit and a bypass system .

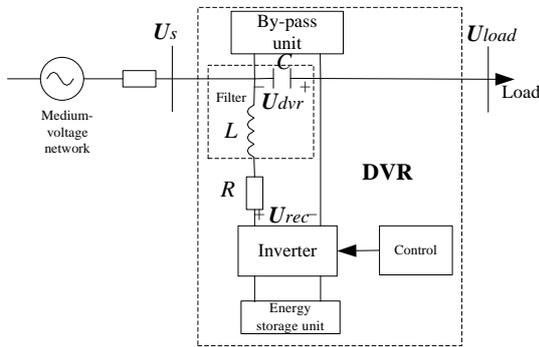


Fig.1 The structure of DVR system

The energy storage devices provide the energy needed by the DVR to compensate the voltage sags and it mainly includes the forms of large capacitor, controllable/un-controllable rectifier with the energy is provided by the grid, superconducting energy storage and other energy storage methods. Inverter transfers the DC energy provided by energy storage devices and produces the compensation voltage as required. Filter unit eliminates the higher harmonic produced by the inverter and couples the inverter to the network.

In Fig.1, every single phase of the inverter of the regional DVR adopts the forms of five cascaded H-bridge, the control system produces SPWM control signal (this system adopts the carrier phase shifting SPWM) to control the inverter to realize the system voltage compensation. Taking one phase for example, u_c represents the voltage of the capacitor, U_{cm} is its peak value, U_d is the inverter output voltage and I_L represents the filter inductor current.

In designing the LC filter, the change of capacitance has little influence on its cost and size, but the change of inductance has large impact, so the key issue is the designing of the value of inductor. The inductor should be to meet the goal of fast current tracking and current ripple suppression. Inductor current is mainly composed of load current and parts of capacitor current, due to the fact that the capacitor current is much less than the load current, so it can be approximate that the inductor

current is equal to the load current when designing.

2 Filter parameters design

2.1 Determination of the value of inductor

Supposing that inductor current i_L is sinusoidal and DVR output power factor is unit. The max change rate of inductor current occurs at the zero-cross point, the inductor value should be small enough to meet the fast current tracking requirements, thereby the upper value limit of inductance can be obtained. When the inductor current reaches the peak, current ripple is the most serious, and the value of inductance should be large enough to suppress the current ripple, thereby the lower value limit of the inductor can be obtained .

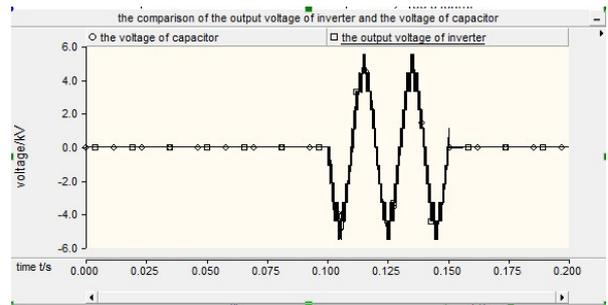


Fig.2 The output voltage waveform of the inverter

Fig.2 is the output voltage waveform of a single-phase of inverter (take phase A as an example). When the inverter uses phase shift carrier PWM, the voltage need to be compensated is generated by the superposition of n cascaded H-bridge. Therefore, the output voltage u_d is between $(n-1)V_{dc}$ and V_{dc} , where V_{dc} is the DC voltage of each H-bridge unit of the inverter.

The peaks of the output current of the inverter in Fig.2 is shown in Fig.3. Suppose the DVR output power factor is $\cos\phi$, and the corresponding output voltage instantaneous value is $U_{cm}\cos\phi$;

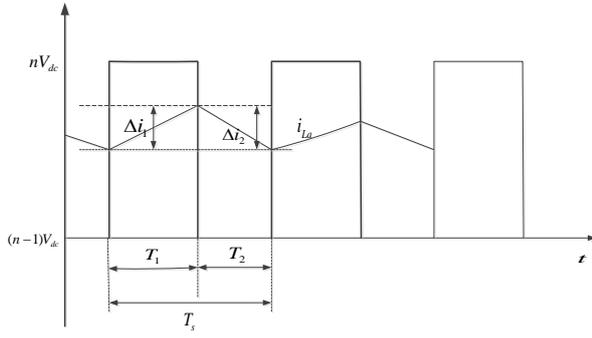


Fig.3 Enlarged waveform of the output voltage under the peak current

In Fig.3, when $0 < t < T_1$, there is:

$$u_d - u_c = nV_{dc} - U_{cm} \cos \varphi \approx L \frac{\Delta i_1}{T_1} \quad (1)$$

When $T_1 < t < T_s$, there is:

$$u_d - u_c = (n-1)V_{dc} - U_{cm} \cos \varphi \approx L \frac{\Delta i_1}{T_2} \quad (2)$$

When the current is at its peak value we can obtain that:

$$|\Delta i_1| = |\Delta i_2|$$

Because of $T_1 + T_2 = T_s$, then T_1 can be solved from equation (1) and (2) as:

$$T_1 = \frac{U_{cm} \cos \varphi - (n-1)V_{dc}}{V_{dc}} T_s \quad (3)$$

And:

$$\Delta i_1 = \frac{(nV_{dc} - U_{cm} \cos \varphi)[U_{cm} \cos \varphi - (n-1)V_{dc}] T_s}{\Delta i_1 V_{dc}} \quad (4)$$

$$L = \frac{(nV_{dc} - U_{cm} \cos \varphi)[U_{cm} \cos \varphi - (n-1)V_{dc}] T_s}{\Delta i_1 V_{dc}} \quad (5)$$

When using the CPS-SPWM modulation, in order to reduce the current ripples effectively, according to formula(5), we can obtain:

$$L \geq \frac{(nV_{dc} - U_{cm} \cos \varphi)[U_{cm} \cos \varphi - (n-1)V_{dc}] T_s}{\Delta i_{\max} V_{dc}} \quad (6)$$

In equation (6), n is determined by $U_{cm} \cos \varphi$ and is an integer closest to $|U_{cm} \cos \varphi| / V_{dc}$. The lower limit value of filter inductor has an relationship with the peak of maximum compensation voltage peak U_{cm} and power factor $\cos \varphi$.

2.2 Determination of the range of capacitance.

Considering the cost and volume demand of the inductance design, we can choose its minimum value which calculated by equation (6). After that, we may design capacitance parameter according to the following method. First, the filter capacitance current can't be too big, or it will increase the cost and the power loss. Second, the effect of the capacitor is to filter the voltage ripple caused by SPWM modulation and lower voltage waveform distortion. At the same time it must guarantee the bandwidth of the LC filter to meet the requirements of voltage tracking speed. The resonance frequency of the LC filter f_r should be greater than the system frequency f_n and less than the PWM switching frequency f_{psw} , i.e.:

$$10f_n \leq f_r = \frac{1}{2\pi\sqrt{LC}} \leq Mf_{psw} \quad (7)$$

In equation (7), the scope of M is $[0.1, 0.5]$. In order to reduce the cost and volume of the DVR filter, under the premise to meet the application requirements, the capacitor should be as small as possible.

3 Simulation verifaciton

The value of designed filters is simulated and verified based on the simulation model shown in Fig.4. The corresponding parameters of 10kV regional dynamic voltage restorer are shown in Table 1.

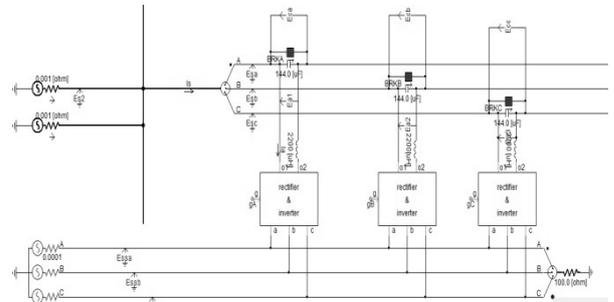


Fig.4 Simulation model of the system including DVR

Table.1 System parameters

System voltage RMS value	10kV
number of single phase cascaded-H Bridge	5
voltage drop depth	0-0.5pu
equivalent switching frequency	5000HZ
(Δi_{\max}) maximum current ripples	23A

According to equation (6), the lower value limit of the filter inductor is the function of $\cos\phi$ and U_{cm} , denotes it as a function $f(U_{cm}, \cos\phi)$. According to system parameters shown in Table.1, the changes of $f(U_{cm}, \cos\phi)$ plotted by using Matlab is shown in Fig.5.

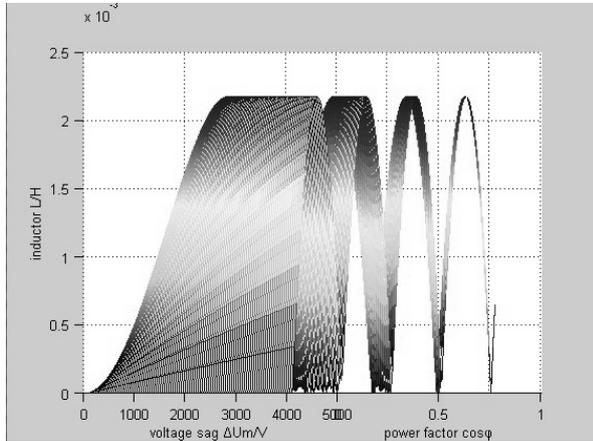
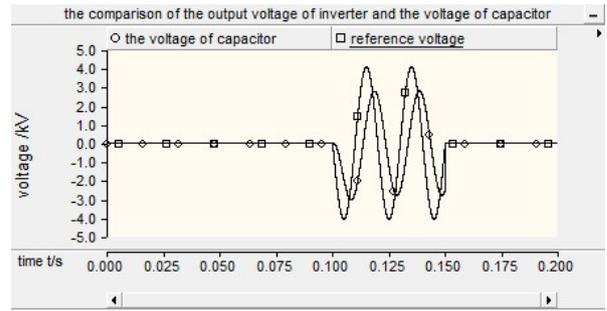


Fig.5 The curve of value of $f(u_{cm}, \cos\phi)$

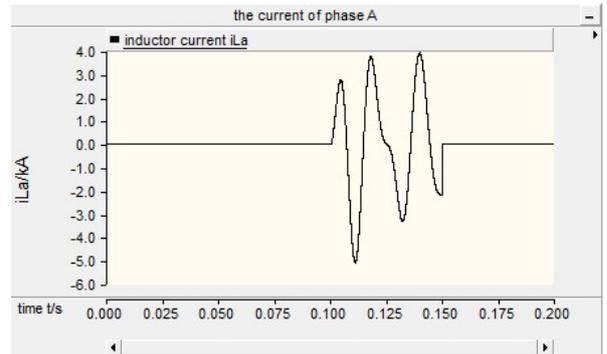
According to Fig.5, the minimum value of function $f(U_{cm}, \cos\phi)$ can be obtained as 2200, which means $L \geq 2200\mu\text{H}$. Taking the size and cost of the filter into consideration, the value of L is then chosen as 2200 μH .

According to equation (7), when the value of M is within $[0.1, 0.5]$, the ranges of capacitance is $1.703\mu\text{F} \leq C \leq 144.76\mu\text{F}$. The actual value of C is 144 μF .

Fig.6-Fig.8 are respectively the DVR output voltage compared with a reference voltage value when filter elements with different value, and the inductor current waveform.

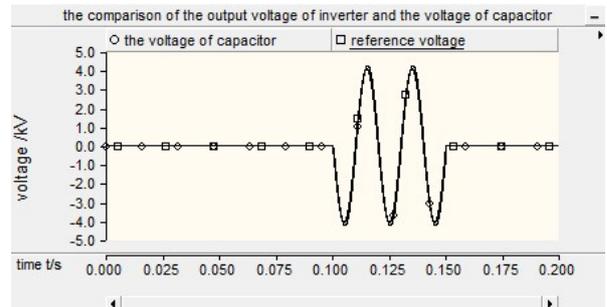


(a) The output and reference voltage of DVR

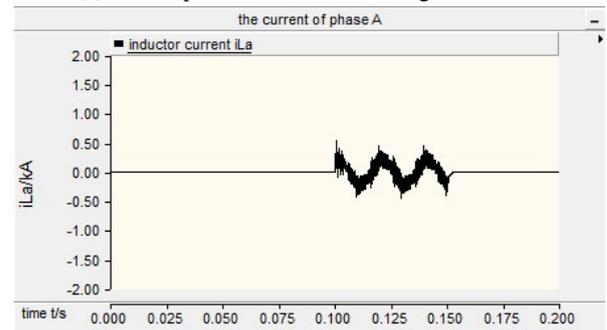


(b) The inductor current

Fig.6 Simulation results when $C=1440\mu\text{F}$ and $L=2200\mu\text{H}$

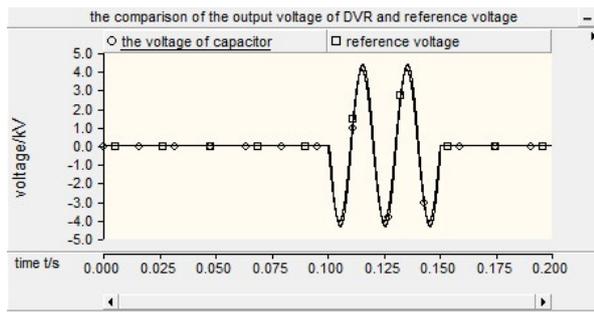


(a)The output and reference voltage of DVR

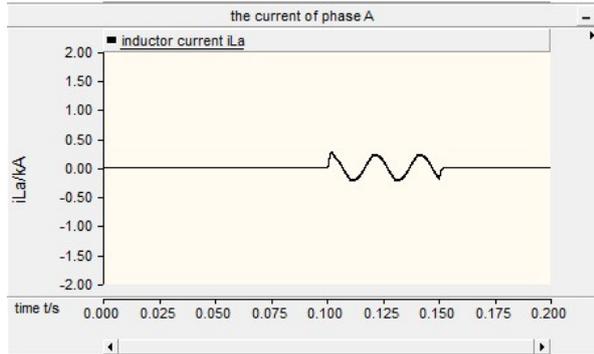


(b)The inductor current

Fig.7 Simulation results when $C=144\mu\text{F}$ and $L=220\mu\text{H}$



(a) The output and reference voltage of DVR



(b) The inductor current

Fig.8 Simulation results when $C=144\mu\text{F}$ and $L=2200\mu\text{H}$

As it can be seen from the simulation results, when the capacitance changes, the difference between DVR output voltage and the reference voltage is bigger, and when inductance changes, the harmonic content of inductor current increases. Therefore, as shown in Fig.8, the value of filter gets ideal results.

4 Conclusion

This paper presents the design of LC filter parameters of regional DVR based on the maximum compensation voltage and inverter output power factor. Through the analysis of inverter output current at the peak value, theoretical expression of the lower value of filter inductor is derived, the capacitance value is determined according to the requirement of filter resonant frequency. Simulation results show that the optimal design of filter parameters fully meets the system performance requirements, and reduce the cost and size of DVR filter. This paper provides a reference for optimal design of large-capacity high-voltage power electronic

device output filter.

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